REMARKS

Claims 1 – 30 remain in the application and stand rejected. Claims 1 and 12 are amended herein. No new matter is added.

Amendments to claims 1 and 12 are supported by the specification as filed and by claim 19. No new matter has been added.

Claims 1 – 5, 7 – 9, 12 – 15, 18 – 23 and 25 – 27 are rejected under 35 U.S.C. §102(b) over U.S. Patent No. 4,786,830 to Foss. Claims 6, 16, 24 and 30 are rejected under 35 U.S.C. §103(a) over Foss. alone Claims 10 and 28 are rejected under 35 U.S.C. §103(a) over Foss in view of E.P. 125,733 to Feller. Claims 11, 17 and 29 are rejected under 35 U.S.C. §103(a) over Foss in view of Kao, "Dual Threshold Voltage Domino Logic." The rejection is respectfully traversed.

Foss teaches a "TTL to CMOS-input buffer." Abstract, line 1, *and see*, the title, col. 1, lines 6 – 43, the first sentence of every paragraph from col. 1, line 46 – col. 3, line 11 and the Foss claims 1 – 8. As far as the applicants are aware, TTL circuits have never been integrated on the same chip with CMOS logic. Thus, the Foss "TTL to CMOS-input buffer" is an input to a CMOS chip that is compatible with TTL levels from external (off chip) TTL chips, i.e., it is a chip input/output (I/O) circuit. *See, e.g.*, column 1, lines 41 – 43. Moreover, the Foss "TTL to CMOS-input buffer" 2 includes "a Schmidt trigger circuit 10 and a first and a second inverter 20 and 30, respectively, each of which is connected to a first and a second power supply terminal V_{CC}, and V_{SS} respectively." Col. 3, lines 11 – 15. The Schmidt trigger circuit 10 output 21 drives the first inverter 20 and the first inverter 20 drives the second inverter 30. *See, e.g.*, Figure 2. The applicants note that Foss indicates that V_{CC} is 5 volts (col. 3, line 7), which was identical to the supply voltage used for TTL logic at the time of filing Foss, 1987. The up level of the Schmidt trigger circuit output 21 is below the supply voltage (V_{CC}) by the threshold

voltage (V_{TH}) of FET 4, i.e., the Schmidt trigger circuit output 21 switches between output levels of 0.0V and V_{CC}-V_{TH4}. However, V_{CC}-V_{TH4} is not a supply level.

Regarding claim 19, it is asserted that "Foss discloses, in Fig. 2, an integrated circuit (IC)(col. 1, lines 7+) comprising: a plurality of circuit rows (inherent since COMOS [sic] input circuits are used in IC; col. 1, lines 7+);" but the recitation of a single TTL compatible I/O circuit says nothing about the organization of any chip that might require TTL compatible I/Os. Regardless, it is further asserted that Foss et al. also discloses "at least one low voltage island (21) in at least one of said plurality of circuit rows, circuit elements (1, 2) in each said at least one low voltage island being powered by a low voltage (Vddl) supply (Vcc-VTH4; col. 3, lines 50+);... ." However, as noted hereinabove, 21 is the Schmidt trigger circuit 10 output, not an island, much less a low voltage island and certainly not a low voltage island with "circuit elements ... powered by a low voltage (V_{ddl}) supply" as claim 19 recites. FETs 1 and 2, are part of the Schmidt trigger circuit 10 and part of the Foss "TTL to CMOS-input buffer." As further noted hereinabove, V_{CC}-V_{TH4} is not a supply level. Thus, although it is asserted that Foss teaches "at least one high voltage island (Vcc) in said at least one of said plurality of circuit rows, circuit elements in each said at least one high voltage island being powered by a high voltage (Vddh) supply (Vcc), Vddb being a higher voltage than Vddl (Vcc > Vcc - VTH4);" Foss teaches a "TTL to CMOS-input buffer" supplied by a single supply voltage, V_{CC}. Therefore, Foss fails to teach the present invention as recited in claim 19. Reconsideration and withdrawal of the rejection of claim 19 under 35 U.S.C. §102(b) over Foss is respectfully requested.

Claim 1 is amended to recite that the level converter interfaces "circuits in the same integrated circuit (IC) as said level converter and supplied by different supply voltages," which is neither taught nor suggested by the Foss I/O circuit or by any reference of record. Claim 12 is amended to recite that the "first inverter with a first inverter input connected to an output of a first circuit on the same integrated circuit (IC)

as said first inverter," and that the second inverter output is "connected to an input of a second circuit on the same integrated circuit (IC) as said second inverter," which is neither taught nor suggested by the Foss I/O circuit or by any reference of record. Therefore, Foss does not teach or suggest the present invention as recited in amended claims 1 or 12. Reconsideration and withdrawal of the rejection of claims 1 and 12 under 35 U.S.C. §102(b) over Feller is respectfully requested.

Furthermore, because dependent claims include all of the differences with the prior art as the claims from which they depend, Feller does not teach or suggest the present invention as recited in any of claims 2 – 9, 13 – 16, 18, 20 – 27, or 30, which depend from claims 1, 12, and 19. Reconsideration and withdrawal of the rejection of claims 2 – 9, 13 – 16, 18, 20 – 27 and 30 under 35 U.S.C. §§102(b) or 103(a) over Foss is respectfully requested.

Regarding the rejection of claims 10 and 28 under 35 U.S.C. §103(a) over Foss in view of Feller and Claims 11, 17 and 29 over Foss in view of Kao, neither Feller nor Kao adds anything to the Foss I/O circuit to result in the present invention as recited in claims 1, 12 or 19, from which claims 10, 11, 17, 28 and 29 depend. Therefore, the present invention as recited in claims 10, 11, 17, 28 and 29 is patentable over the combination of Foss with Feller, Kao or any reference of record. Reconsideration and withdrawal of the rejection of claims 10, 11, 17, 28 and 29 under 35 U.S.C. §103(a) over Foss in combination Feller or Kao with is respectfully requested.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance both for the amendment to the claims and for the reasons set forth above, the applicants respectfully request that the Examiner reconsider and withdraw the rejection of claims 1 – 30 under 35 U.S.C. §§102(b) and 103(a) and allow the application to issue.

Should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-0510 and advise us accordingly.

Respectfully Submitted,

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(Date)

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